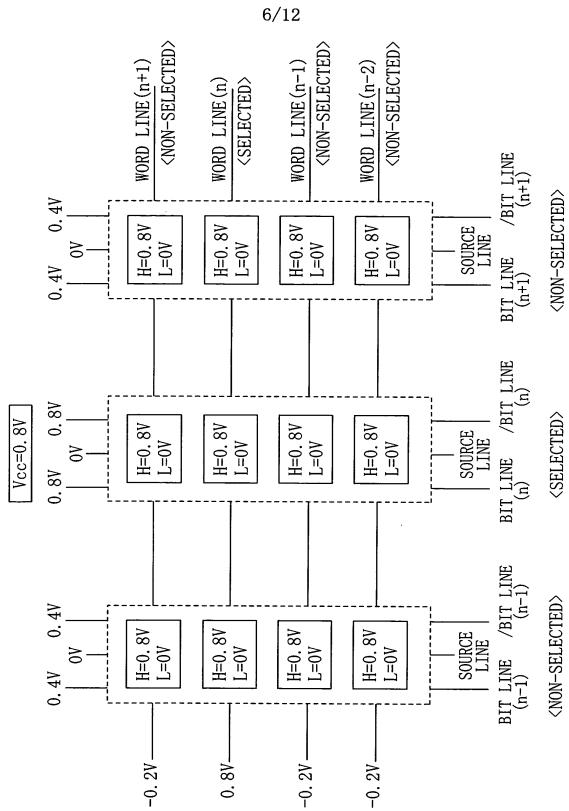


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		LARGE NEGATIVE VOLTAGE	INTERMEDIATE NEGATIVE	SMALL NEGATIVE VOLTAGE
		$(-Vcc\sim -Vcc/2)$	$(-V_{cc}/3\sim -V_{cc}/4)$	$(-V_{cc}/6\sim 0V)$
NON- SELECTED	OFF LEAKAGE CURRENT	VERY SMALL	INTERMEDIATE	VERY LARGE
WOKD LINE	GATE LEAKAGE CURRENT	VERY LARGE	INTERMEDIATE	SMALL
VOLTAGE /	GIDL LEAKAGE CURRENT	VERY LARGE	INTERMEDIATE	SMALL
		HIGH POTENTIAL PRECHARGE	INTERMEDIATE POTENTIAL PRECHARGE	LOW POTENTIAL PRECHARGE
		(Vpre=Vcc)	(Vpre=Vcc/2)	$(\text{Vpre=Vcc/3}\sim 0\text{V})$
NON- SELECTED	OFF LEAKAGE CURRENT	INTERMEDIATE	SMALL	INTERMEDIATE
BII LINE	GATE LEAKAGE CURRENT	LARGE	SMALL	LARGE
VOLTAGE / SOURCE /	GIDL LEAKAGE CURRENT	LARGE	SMALL	LARGE
-NON		HIGH POTENTIAL LOW LEVEL (Vsn=Vcc/2)	INTERMEDIATE POTENTIAL LOW LEVEL (Vsn=Vcc/4)	LOW POTENTIAL LOW LEVEL (Vsn=0V)
SELECTED SOURCE	OFF LEAKAGE CURRENT	VERY SMALL (DATA RETENTION UNSTABLE)	INTERMEDIATE	LARGE
/ OSN /	GATE LEAKAGE CURRENT	UNRELATED (DATA RETENTION UNSTABLE)	UNRELATED	UNRELATED
VOLTAGE / SOURCE /	GIDL LEAKAGE CURRENT	VERY SMALL (DATA RETENTION UNSTABLE)	INTERMEDIATE	SMALL

FIG. 5

	STATE	VOLTAGE SOURCE	SELECTED	NON-SELECTED
	Mode-A	NWL VOLTAGE SOURCE (WORD LINE)	Vcc	-1/3 Vcc
DURI	HIGH /	HPR VOLTAGE SOURCE (BIT LINE)	1/2 Vcc~Vcc	1/2 Vcc
NG C	(IEMPEKAIUKE/	OSN VOLTAGE SOURCE (SOURCE LINE)	Vss	1/3 Vcc
PERA	Mode-B	NWL VOLTAGE SOURCE (WORD LINE)	Vcc	-1/4 Vcc
TION	/LOW TO ROOM/	HPR VOLTAGE SOURCE (BIT LINE)	1/2 Vcc~Vcc	1/2 Vcc
I	(TEMPERATURE)	OSN VOLTAGE SOURCE (SOURCE LINE)	Vss	1/4 Vcc
	Mode-C	NWL VOLTAGE SOURCE (WORD LINE)		-1/3 Vcc
DUR	HIGH	HPR VOLTAGE SOURCE (BIT LINE)		floating
ING	(IEMPEKATUKE)	OSN VOLTAGE SOURCE (SOURCE LINE)		1/3 Vcc
STAN	Mode-D	NWL VOLTAGE SOURCE (WORD LINE)		-1/4 Vcc
DBY	/LOW TO ROOM/	HPR VOLTAGE SOURCE (BIT LINE)		floating
	(TEMPERATURE)	OSN VOLTAGE SOURCE (SOURCE LINE)		1/4 Vcc



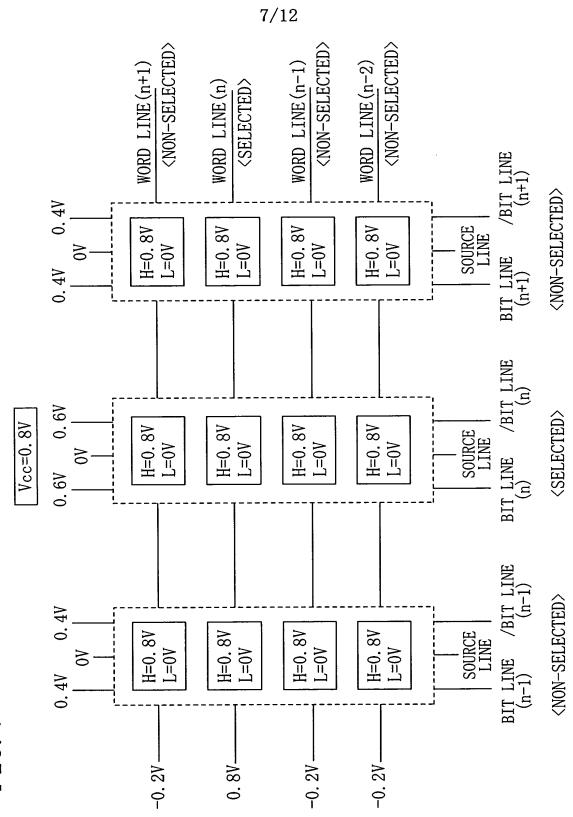


FIG. 8

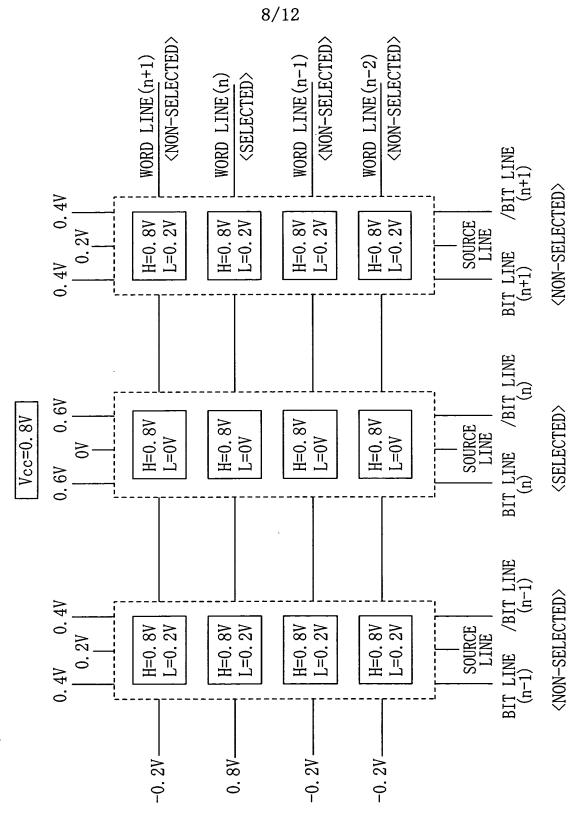


FIG. 9

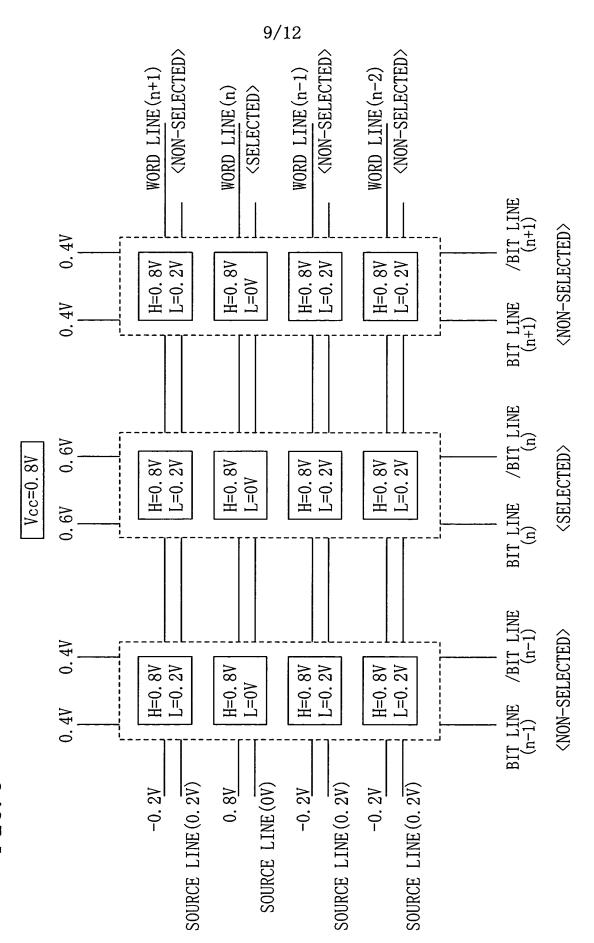
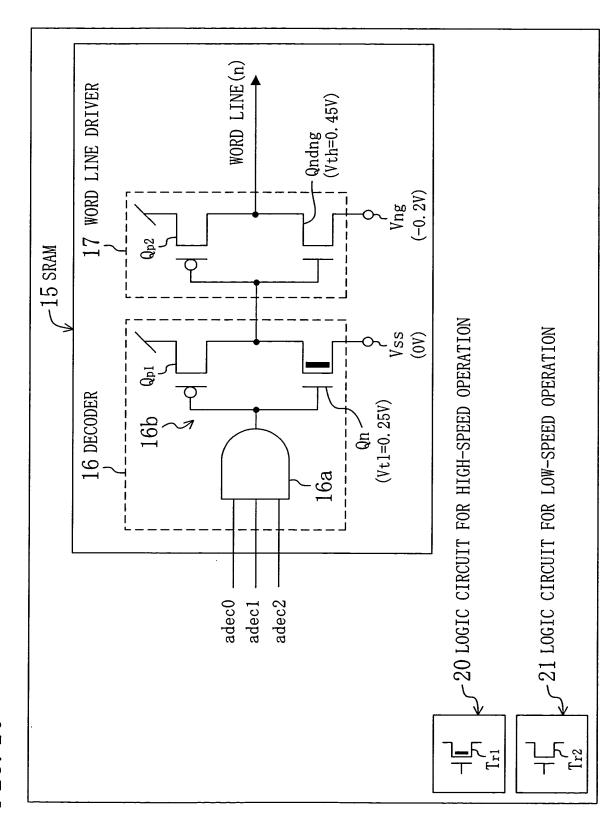


FIG. 10



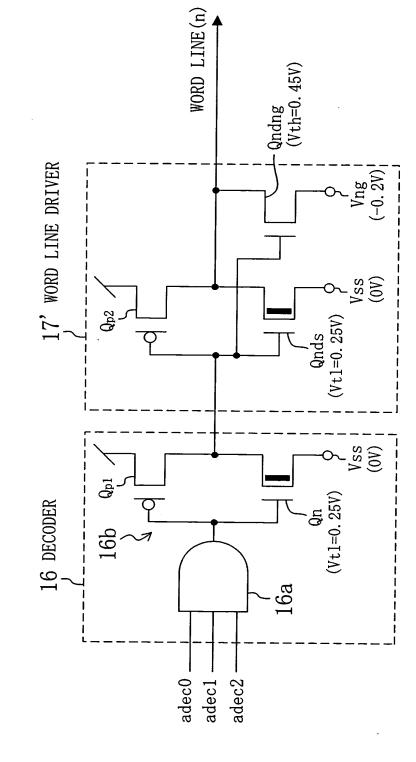


FIG. 11

FIG. 12

